CMOS ACTIVE PIXEL IMAGE SENSORS FOR HIGHLY INTEGRATED IMAGING SYSTEMS

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ABSTRACT

A family of CMOS-based active pixel image sensors (APS) that are inherently compatible with the integration of on-chip signal processing circuitry is reported. The image sensors were fabricated using commercially available 2 μm CMOS processes and both p-well and n-well implementations were explored. The arrays feature random access, 5V operation and TTL compatible control signals. Methods of on-chip suppression of fixed pattern noise to less than 0.1 % saturation are demonstrated. The baseline design achieved a pixel size of 40 μm x 40 μm with 26% fill-factor, Array sizes of 28 x 28 elements and 128 x 128 elements have been fabricated and characterized. Typical output sensitivity is 3.7 μV/e⁻ for the p-well devices and 6.5 μV/e⁻ for the n-well devices. Input referred read noise of 28 e⁻ r.m.s. corresponding to a dynamic range of ’76 dB was achieved, Characterization of various photogate pixel designs and a photodiode design is reported. Intra-pixel photoresponse maps taken using a focused laser scanning apparatus arc presented.

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I. INTRODUCTION

In many imaging systems, integration of the image sensor with circuitry for both driving the image sensor and performing on-chip signal processing is becoming increasingly important, A high degree of electronics integration on the focal-plane can enable miniaturization of instrument systems and simplify system interfaces. In addition to good imaging performance with low noise, no lag, no smear and good blooming control, it is desirable to have random access, simple clocks and fast read out rates. The development of a CMOS-compatible image sensor technology is an important step for highly integrated imaging systems since CMOS is well-suited for implementing on-chip signal processing circuits. CMOS is also a widel y accessible and well -understood technology.

Charge-coupled devices (CCDs) are currently the dominant technology for image sensors. CCD arrays with high fill-factor, small pixel sizes and large formats have been achieved and limited signal processing operations have been demonstrated with charge-domain circuits [1,2]. However, CCDS cannot be easily integrated with CMOS circuits due to additional fabrication complexity and increased cost. Also, CCDs arc high capacitance devices so that on-chip CMOS drive electronics would dissipate prohibitively high power levels for large area arrays (2-3 W). Furthermore, CCDS need many different voltage levels to ensure high charge transfer efficiency. The readout rate is limited due to the inherent sequential read out of CCDS and the need to achieve nearly perfect charge transfer efficiency to maintain signal fidelity. CCDS also suffer from smear and susceptibility to radiation damage.

An active pixel image sensor is defined as an image sensor technology that has one or more active transistors within the pixel unit cell [3]. Previously demonstrated active pixel sensor (APS) technologies include the amplified MOS imager (AMI) [4], charge modulation device (CMD) [5], bulk charge modulated device (BCMD) [6], base stored image sensor (BASIS) [7] and the static induction transistor (SIT) [8]. Although AMIs are both CMOS-compatible and amenable to integration with on-chip circuitry, high noise levels and lag are a problem. CMDS, BCMDS and BASIS are also amenable to integration with on-chip circuitry, but can be made CMOS-compatible only with additional fabrication steps. SITs are difficult to integrate with on-chip circuitry and arc not CMOS-compatible.

The CMOS active pixel sensors described in this paper are inherently CMOS-compatible. Each pixel unit cell contains an imaging element and three transistors for readout, selection and reset. A column parallel architecture is used for readout and the imager is read out a row at a time. The two major innovations reported in this paper are the use of intra-pi xel charge transfer to allow correlated-double-sampling (CDS) and on-chip fixed pattern noise (FPN) suppression circuitry located in each column. These innovations will allow, for the first time, a CMOS APS to achieve low noise performance comparable to a CCD. In all the designs random access is possible, allowing selective readout of windows of interest. The image sensors are operated with TTL clocks and at most two other d.c. voltages. These image sensors

achieve lateral blooming control through proper biasing of the reset transistor. No lag or smear is evident. The reset and signal levels arc read out differentially, allowing CDS to eliminate kTC noise, l/f noise and fixed pattern noise from the pixel. Low noise and high dynamic range are achieved. The option of using a radiation hard CMOS process is also available. The CMOS active pixel image sensors reported here have performance suitable for many applications including robotics and machine vision, guidance and navigation, automotive applications, and consumer electronics such as video phones, computer inputs and home surveillance devices. Future development will lead to scientific sensors suitable for highly integrated imaging systems for NASA deep space and planetary spacecraft.

This paper presents the design and performance of a family of CMOS active pixel image sensors. Section II describes the baseline design, its operation and noise analysis. Section III presents two fixed pattern noise suppression methods that were investigated. The experimental results of the baseline design and FPN suppression schemes are presented in Section IV. Section V describes the different pixel unit cell designs explored and compares their performance with the baseline design.

11. THE BASELINE CMOS APS

A. *Design*

A schematic of the baseline pixel design and readout circuit used in the CMOS APS arrays is shown in Fig. 1(a). The pixel unit cell is shown within the dotted outline. The imaging structure consists of a photogate (PG) with a floating diffusion output (FD) separated by a transfer gate (TX). In essence, a small surface-channel CCD has been fabricated within each pixel. The pixel unit cell also contains a reset transistor (MR), the input transistor of the in-pixel source-follower (MIN) and a row selection transistor (MX).

The readout circuit which is common to an entire column of pixels includes the load transistor of the first source-follower (MLN) and two sample and hold circuits for storing the signal level and the reset level, Sampling both the reset and signal levels permits correlated double sampling (CDS) which suppresses reset noise from the floating diffusion node of the pixel, and I/f noise and threshold variations from the source-follower transistor within the pixel [9]. Each sample and hold circuit consists of a sample and hold switch (MSHS or MSHR) and capacitor (CS or CR) and a column source follower (MP1 or MP2) and column selection transistor (MY1 or MY2). The load transistor of the column source-followem (MLP1 and MLP2) are common to the entire array of pixels. The transistor and capacitor sizes are summarized in table I.

R. Operation

The operation of this image sensor is illustrated in Figs. 2(a)-(d), The rail voltages VDD and VSS are set at 5V and OV respectively, and the transfer gate TX is biased at 2.5V. The load transistors of the in-pixel source-follower and the column source-followers (MLN, MLP1 and MLP2 in Fig. 1(a)) arc d.c.

biased at 1.5V and 2.5V respectively. During the signal integration period (Fig. 2(a)), photo-generated electrons are collected under the surface-channel photogate PG biased at 5V. The reset transistor MR is biased at 2.5V to act as a lateral anti-blooming drain, allowing excess signal charge to flow to the reset drain. The row-selection transistor MX is biased off at 0V. Following signal integration, an entire row of pixels arc read out simultaneously. First, the pixels in the row to be read out are addressed by enabling row selection switch MX. Then the floating diffusion output node of the pixel (FD) is reset by briefly pulsing the reset gate of MR to 5V. This resets FD to approximately 3.5V (Fig. 2(b)). The output of the first source follower is sampled onto capacitor CR at the bottom of the column by enabling sample and hold switch MSHR. Then, PG is pulsed low to OV, transferring the signal charge to FD (Fig. 2(c)). The new output voltage is sampled onto capacitor CS by enabling sample and hold switch MSHS (Fig. 2(d)). The stored reset and signal levels arc sequentially scanned out through the second set of source followers by enabling column address switches MY 1 and MY2. This timing sequence is shown in Fig. 1(b).

C. Noise analysis

The main noise sources associated with this system arc reset noise on the floating diffusion node, I/f noise from the input transistor of the in-pixel source-follower, dark current shot noise, reset noise on the sample and hold capacitors, and white noise and I/f noise from the second source-follower.

The column CDS operation suppresses reset noise on the floating diffusion node within the pixel. Considering the frequency response of the in-pixel source-follower, the output referred post-CDS reset noise power can be expressed as

$$\left\langle v_{FD}^2 \right\rangle = A_1^2 A_2^2 \frac{kT}{C_{FD}} \left[e^{-2\pi f_{c1} t_r} \left(1 - e^{-2\pi f_{c1} t_s} \right) \right] \qquad (1)$$

where A_1 and A2 are respectivel y the gains of the in-pixel and column source-follo wers, C_{FD} is the capacitance of the floating diffusion node, t_r and t_s arc as shown in Fig. 1(b) and f_{c1} is the cutoff frequency of the in-pixel source-follower. The output referred l/f noise power associated with the in-pixel source-follower can be expressed as

$$\left\langle v_{f1}^2 \right\rangle = 4\alpha_1 A_1^2 A_2^2 \left[0.577 + \ln\left(2\pi f_{c_1} t_s \right) \right] \qquad (2)$$

where al is the flicker noise coefficient of the in-pixel source-follower input transistor (MIN) [10]. Dark current shot noise from each pixel can be expressed in output referred noise power as

$$\left\langle v_{dk}^2 \right\rangle = A_1^2 A_2^2 \frac{I_{dark} \Delta t}{C_{FD}^2} q \qquad (3)$$

where I_{dark} is the pixel dark current and At is the integration time. Output referred photon shot noise power can be written as

$$\left\langle v_{ph}^2 \right\rangle = A_1^2 A_2^2 \frac{I_{photo}\Delta t}{C_{FD}^2} q \qquad (4)$$

where I_{photo} represents the input signal.

The reset noise on each sample and hold capacitor is due to the white noise in the in-pixel source-follower and the sample and hold switches. The output referred reset noise power is given by

$$\left\langle v_{rsh}^2 \right\rangle = 2 A_2^2 kT \left(\frac{1}{C_S + C_B} + \frac{1}{C_S} \right) \qquad (5)$$

where C_S and C_B arc respectively the sample and hold capacitance and the column output bus capacitance, The prefactor of 2 represents noise contribution from the two sample and hold branches. The noise introduced by the column source-followers is given by

$$\left\langle v_{n2}^2 \right\rangle = 2 \frac{kT}{C_{out}} + 8\alpha_2 A_2^2 \left[0.577 + \ln\left(2\pi f_{c_2} t_c \right) \right] \qquad (6)$$

where C_{out} is the effective load capacitance at the output of the column source-followers, α_2 is the flicker noise coefficient of the column source-follower input transistors (MP1 and MP2), f_{c2} is the cutoff frequency of the column source-follower and t_c is the time from sampling to readout. The first term represents the white noise cent ribution and the second term represents the l/f noise component.

In addition to the temporal noise described above, another important source of noise in the image sensor is the fixed pattern noise caused by threshold voltage variations in transistor in the readout circuit.

111. FIXED PATTERN NOISE SUPPRESSION

In the baseline CMOS APS &sign, fixed pattern noise (FPN) can limit performance of the sensor so that reduction of FPN is essential for improvement of image quality. FPN is dominated by column-to-column variations due to the column parallel readout structure. The origin of the column-wise FPN is believed to be threshold voltage variations between the pair of adjacent p-channel source-follower input transistors in the readout circuits located at the bottom of each column. FPN can therefore be greatly reduced by eliminating or reducing the offsets in the column processing circuitry. Two techniques of FPN suppression are presented below.

A. Subtracting a column reference

The first method uses computer software to subtract a dark reference voltage from the signal. The reference for each column is obtained from the last row of pixels in the array, which is covered by light shield. This approach can be implemented on-chip if desired. Of course, an entire dark image can be subtracted from an acquired image for greater FPN suppression, but this requires acquisition and storage of the dark image,

B. Crowbar circuit

The second column-FPN suppression scheme utilizes additional switches to measure the offset in each column. Fig. 3(a) is a schematic of the baseline APS design with the output circuit modified to incorporate the FPN suppression scheme. In each column output circuit, a crowbar switch (CB) and two column selection switches on either side (MS 1 and MS2) were added to selectively short the two sample and hold capacitors CS and CR. The image sensor is operated as described previously up to the sampling of the reset and signal levels onto the two sample and hold capacitors (Fig. 3(b)). However, during the scanning of the columns, an additional step is performed. After differentially reading out the reset and signal levels stored in each column (A 1), the crowbar switch is pulsed, thereby shorting the two sample and hold capacitors in the column that is being addressed. The outputs of the reset and signal branches are again read out differentiall y, thereby generating a voltage which is proportional to the threshold voltage difference between the two adjacent transistors ($\Delta 2$). By subtracting this reference level from the previous reading, the offset duc to threshold voltage variations is removed ($\Delta' = \Delta 1 - \Delta 2$).

IV. EXPERIMENTAL RESULTS

The CMOS APS designs reported in this paper were fabricated using double-poly, double-metal CMOS processes with 2pm design rules. The resulting pixel size was 40 µm x 40 pm. The baseline design was first implemented using a p-well CMOS technology as a 28 x 28 element test array (AR28P2) and later expanded to a 128 x 128 element array (AR128P2) and an n-well implementation (AR128N2). A microphotograph of a completed 128 x 128 element CMOS APS array is shown in Fig. 4. The row decoders and clock generator circuits to the left of the APS array and the column decoders and readout circuits below the APS array were designed to fit within the 40pm pixel pitch. The 7-bit row and column address decoders were formed using standard CMOS logic permitting direct X-Y addressing of' the image sensor. The circuitry out.side the pixel array is covered by a light shield fabricated using swond-level metal. Thc 28x 28 element test arrays were also designed with the same chip architecture. The die areas of the large and small arrays were 6.8 mm x 6.8 mm and 2.22 mm x 2.25 mm respectively. The pixel unit cell and readout circuits were designed to achieve 30 Hz frame rate operation of a 128 x 128 element array.

Two modes of operation were used to characterize the CMOS active pixel image sensors. In video rate operation, the image sensor was operated at a 30 Hz frame rate and a scan converter and video monitor were used to display the output image. In the data acquisition mode, image data was captured using a 100 kHz 16-bit ADC and displayed on a computer screen. The resulting frame rate was 5 Hz and the measured system noise was approximately 25 µV r.m s.

A. Baseline CMOS APS

The active pixel image sensors were operated with the timing and voltages described in Section II. However, in the n-well image sensors, the load transistor of the in-pixel source follower (MLN) was biased

at 1.25 V. Higher biasing made the column amplifiers "glow" and saturate the lower region of the image sensor array. This effect can be reduced by switching off column selection transistors MY 1 and MY2, and load transistor MLN in all the columns during long integration periods. Both dark and illuminated testing of the sensors were performed. Pixel output sensitivity is determined by measuring the ratio of the variance to the mean of the output signal over many frames, for a given pixel, assuming photon shot-noise limited performance. The measured pixel output sensitivity was 3.7 $\mu V/e^-$ for the p-well design and 6.5 $\mu V/e^-$ for the n-well design. These results were confirmed by performing electrical tests on a test structure on a separate IC. In the test structure, the sensitivity at the output of the in-pixel source follower was measured to be 4.0 $\mu V/e^-$ for the p-well design and 7.0 $\mu V/e^-$ for the n-well design. The higher sensitivity of the n-well design can be attributed in part to lower capacitance of the floating diffusion output node in the n-well process than in the p-well process. Although the photogate full-well capacity was calculated to be approximately 6 x 10^6 e-, saturation was determined by the output amplifier biasing. The observed saturation level was 600 mV corresponding to 162,000 e^- for the p-well design and 1.2V corresponding to 185,000 e^- for the n-well design. Higher saturation levels can be easily achieved by operating the image sensors with a higher supply voltage. For example, by increasing the supply voltage to 6V, the saturation level in the p-well design was increased to approximatel y 1.1 V corresponding to 297,000 e-. The responsivit y (V/W) of the n-well image sensor was approximately 4 times that of the p-well sensor.

For video rate operation (30 Hz frame rate) the sensors were nominally clocked at 2 µs/pixel. For 5V operation, power dissipation was measured to be approximate] y 7 mW for the 128 x 128 element arrays and 5.9 mW for the 28 x 28 element arrays, The major power dissipation was in the p-channel transistor (87%) compared to the column-parallel n-channel transistors (13%). Low power operation of the test array was demonstrated with a supply voltage of 3V. The power dissipation was 0.84 mW and the sat uration level was 200 mV for this mode of operation. The 128 x 128 element array was successful] y operated at over a 70 Hz frame rate, despite its 30 Hz design.

In both the p-well and n-well implementations, no lag or smear was observed. Blooming was suppressed through proper biasing of the reset transistor MR. Dark current of the p-well design was measured to be approximately 0.26 V/s, or under 1 nA/cm^2. Dark current in the n-well design was higher at approximately 1.76 V/s. The higher responsivity and dark current in the n-well designs can be attributed to the increased collection depth and lower floating diffusion capacitance. In the p-well designs, the well depth of approximately 2pm limits the carrier generation depth. In addition, the well depth is small compared to the pixel dimensions of 40 µm x 40 pm. Therefore, electrons that are generated in the well outside a photogate area are more likely to diffuse to the n-substrate than be collected under a photogate. In the n-well designs, electrons that are generated in the substrate Mow a photogate can be collected by that pixel or diffuse to adjacent pixels. This phenomenon also results in higher crosstalk in the n-well designs than the p-well designs

Laser spot scans of individual pixels at 632.8 nm and 488 nm confirmed both higher response and higher crosstalk in" the n-well designs than the p-well designs. The pixel layout of the baseline pixel is shown in Fig. 5(a) for comparison with the responsivity maps, The 632.8 nm Hc-Ne laser had a beam diameter of approximately 1.5 µm and a step size of approximately 2 pm, The responsivity maps of the p well and 'n-well pixel are presented in Fig, 5(b) and 5(c) respectively. In the p-well design, the response is uniform across the photogate area with only poly 1 and drops off rapidly at the edges. A lower response is noticeable in areas overlapped by poly2 or metal. In the n-well design, the response drops off more gradually, and crosstalk from adjacent pixels is evident. These effects increase the effective fill-factor of the pixel. The responsivity maps at 488 nm showed similar patterns. However, the green response was lower than the red response due to the polysilicon photogate.

B. Noise Performance

Noise in the image sensors was measured by averaging the variance of each pixel output over many dark frames. Dark current shot noise was eliminated in this measurement by resetting each pixel before data was acquired, For typical operation of the image sensors, the pixel floating diffusion reset noise suppression through CDS is estimated to be over 8 orders of magnitude. Based on measured flicker noise coefficients, the output referred l/f noise of the in-pixel source-follower was estimated to be approximate y 111 µV r.m.s.. The theoretical reset noise on each 1 pF sample and hold capacitor is 65 µV, resulting in 93 µV for differential mode. The noise introduced by the column source-followers is estimated to be approximately 46 µV for differential mode for a load capacitance of 2.5 pF resulting in a total theoretical noise of approxim atel y 152 µV. The calculated read noise in the column circuit alone excluding the pixel is approximatel y 86 µV. The measured noise level at a 5 Hz frame rate at room temperature was approximately 153 µV. Accounting for system noise, read noise in the p-well image sensor is determined to be 151 µV which is in good agreement with the predicted value. By sampling the pixel reset level onto both sample and hold capacitors, noise in the column readout circuit was measured to be 120 µV. Using measured sensitivity values, the total input referred noise is determined to be 41 e r.m.s. corresponding to a dynamic range of 72 dB.

In order to reduce reset noise, the sample and hold capacitors of the n-well 128 x 128 element army were increased to approximate y 2.3 pF by using an MOS capacitor under the poly 1 -pol y2 capacitor, The theoretical reset noise for this circuit is reduced to 63 µV for differential mode. The total noise is calculated to be 169 µV. Although the reset noise is lower than in the p-well design, the total noise is higher due to a higher flicker noise coefficient observed in the n-well design. The noise in the column circuit is calculated to be 65 µV. The measured noise level at a 5 Hz frame rate at room temperature was approximately 209 µV. Accounting for system noise, the total read noise in the n-well image sensor is determined to be 207 µV and the column circuit noise is determined to be 60 µV. The total input referred

noise is 32 e⁻r.m s. corresponding to a dynamic range of 75 dB. The measured noise levels confirm the predicted relative contributions from the pixel and column noise sources.

C. FPN Suppression

A raw output image from the 128x 128 element p-well image sensor is shown in Fig. 6(a). The faint vertical streaks in the image indicate that FPN is dominated by column to column variations. In the p well designs, global FPN observed in the differential output signal was approximately 20 mV p-p (3.3% sat.), with a local variation of approximately 8 mV p-p (0.8% sat.). The global variation is attributed to poor control of the p-well potential towards the center of the array since slower clocking rates reduced the effect, and the 28 x 28 element array showed a similar but much smaller effect, Fig, 6(b) demonstrates the improvement in image quality over Fig. 5(a) when FPN suppression through subtracting a column reference is used. With this method of FPN suppression, the measured global FPN reduces to 0.8% sat. In the n-well image sensor, global FPN observed in the differential output signal was approximately 30 mV p-p (2.5% sat,). Subtracting a column reference reduced the FPN to 10 mV p-p (0.8% sat.).

The crowbar column-FPN suppression scheme was incorporated into a subsequent n-well design (AR28NCB). The image sensor was operated as described in Section 111, Oscilloscope photos of the output without and with the crowbar operation are shown in Figs. 7(a) and 7(b) respectively. Global FPN of approximately 10 mV was reduced to approximate] y 1 mV with the crowbar operation. Since the saturation in this image sensor was 1,3V, the FPN is reduced from 0,8% sat, to less than 0.08% sat. This reflects a 20 dB reduction in FPN. The output sensitivity was determined to be 7.1 μV/e⁻ and the measured noise level was 197 μV. Input referred read noise was 28 e⁻r.m.s. corresponding to a dynamic range of 77 dB. The crowbar readout circuit was also implemented as an n-well 128x 128 element array (AR128N5). Global FPN of approximately 20 mV (1.8% sat.) was reduced to 3 mV (0.27% sat,) with the crowbar operat ion.

V. OTHER CMOS APS DESIGNS

Variations of the baseline CMOS APS pixel design were investigated and fabricated using commercial CMOS processes, in addition to normal characterization of the 28 x 28 element image sensors, laser spot scans of individual pixels were performed at 632.8 nm. Pixel designs and experimental results are presented below and summarized in table II. Since the ICs were fabricated at different times, some variation in operating characteristics can be expected.

A. Light shielded pixel (APSG2)

A pixel design with light shield covering the entire pixel except the photogate to limit crosstalk was fabricated using a p-well CMOS process (Fig. 8(a)). The responsivity was similar to the p-well baseline design, but showed a steeper drop off at the edge of the photogate area and no detectable response in the

area covered by the light shield, The saturation level was 800 mV and the output sensitivity was determined to be 3.0 μV/e⁻. The measured noise was 168 μV, similar to the other p-well designs.

R. Square photogate pixel (APSG4)

A pixel design with a square photogate which achieved a fill-factor of 18% was demonstrated (Fig, 8(b)) as a p-well array. The baseline design was optimized for high fill-factor, which resulted in an L-shaped photogate area. However, a pixel with a regular photogate structure is more suitable for usc with microlenses which can increase the effective fill-factor to over 70% [11]. A square pixel is also more suitable for centroiding algorithms, The sensitivity of the square photogate pixel was determined to be 3.1 μV/e⁻. The full-well capacity of the square pixel was calculated to be approximately 3.7 x 10^6 e-, but similar to the baseline design, saturation was limited to approximatel y 132,000 e⁻ by the output amplifier biasing,

C. Tiny photogate pixels (APSG1 and APSG7)

A minimum size photogate design of 3 μm x 4pm with a fill-factor of 0.75% was investigated (Fig. 8(c)). Typical diffusion length for electrons in these devices is of the order of centimeters, Therefore, it is possible for photo-generated charge outside the photogate area to diffuse towards the photogate and be collected. Since the blue response is attenuated by the photogate, it was hoped that the open area within the pixel with a minimum size photogate would improve the blue response. Although the photogate area is less than 3% of the baseline design, the responsivity of the n-well tiny photogate pixel (APSG7) was measured to be approximately 42% of the baseline p-well design and approximately 11 % of the n-well design, The saturation level was 500 mV and the sensitivity was determined to be 6 μV/e⁻. The measured noise level was 168 μV. The full-well capacity for this design was approximatel y 175,000 e⁻ which is still higher than the saturation limit determined by the output amplifier biasing. Due to the effect of the p-well depth described in section IV-A above, no significant response was observed outside the photogate area in the p-well design (APSG 1). In this design, the saturation level and sensitivity y were 400 mV and 2.8 μV/e⁻ respective] y.

D. Single-poly pixel (APSG1O)

An n-well pixel with a fill-factor of 12% was implemented as a single-poly design (Fig. 8(d)). This design was investigated as single-poly CMOS processes are more commonly available in sub-micron technologies than double-poly processes. The floating diffusion between the photogate and transfer gate adds kTC noise and marginally increases lag. The sensitivity of the single-poly pixel was determined to be 7.1 μV/e⁻ and the saturation level was 1 V. The measured noise level was 180 μV. Although the photogate area is reduced due to the single-poly design, responsivity is comparable to the baseline design.

E. Photodiode pixel (APSG5)

A photodiode pixel with the same output structure as the above circuits was demonstrated in a p-well process (Fig. 9(a)), This pixel design achieved a till-factor of 35%. Since the output node is the same as the signal charge collection area, it is not possible to reset the output node before readout to eliminate kTC noise by CDS as in the photogate designs. However, by resetting the photodiode after readout and using that reset level for CDS, it is possible to eliminate l/f noise and fixed pattern noise from the pixel. The capacitance of the photodiode node is higher than the capacitance of the output node of the photogate designs, resulting in lower sensitivity. The sensitivity of the photodiode pixel was determined to be approximately *2.1* μV/e⁻. Although the sensitivity is lower, the signal level was approximately 5 times higher than in the p-well baseline photogate design at the same illumination due to the improved optical fill-factor and elimination of the photogate. Thus, the signal-to-noise ratio is improved although absolute noise is increased. The saturation level was observed to be approximately 1,3 V. Fixed pattern noise was approximatel y 7 mV p-p or less than 0.6% sat. Measured noise was 177 μV. Laser spot scans at 632,8 nm and 488 run (Figs. 9(b) and 9(c)) show improved optical response over the photogate designs, Functionally similar to the AMI sensor, the photodiode APS is simpler to scale to smaller design rules and may be preferable for many applications.

VI. CONCLUSIONS

The development of several CMOS-breed image sensors has been presented. Good blooming control was achieved and no lag or smear was observed. Both on-chip and off-chip column-FPN reduction schemes were explored, Global FPN was reduced to less than 0.190 using the on-chip crowbar circuit. In general, n-well designs showed higher sensitivity and saturation levels than p-welt designs which can be attributed in part to lower capacitance of the floating diffusion output node in the n-welt process than in the p-well process. P-well designs showed lower responsivity and no crosstalk between pixels due to the well depth. N-well designs showed higher responsivity but also showed some crosstalk. Since the noise levels were also higher in the n-well designs, dynamic range was comparable to the p-well designs. Various pixel designs optimized for limiting crosstalk, integration with microlenses, improving optical response and use of single-poly CMOS processes have been investigated.

Improved readout schemes and methods to further reduce FPN are currently being investigated. Integration of on-chip analog-to-digital conversion is being explored [12]. Use of 0.8 μm and 1.2 μm CMOS technology can result in higher fill-factor or smaller pixel sires, Tbc use of microlenses can likely improve the effective fill-factor. Larger formats can be implemented with only slight modifications to the readout circuits. High frame rate imaging is also possible with modified transistor sizing and multi-port readout. This ongoing research work paves the way for the development of more complex pixel structures and the integration of more sophisticated on-chip electronics in the future.

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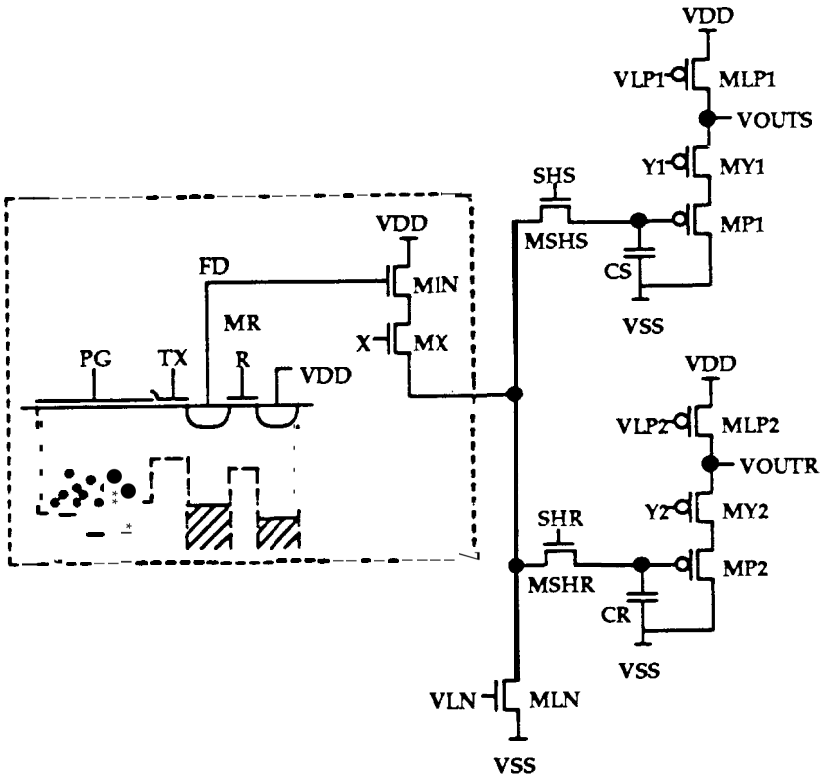
LIST OF TABLES AND FIGURES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MLP1
VOUTS
Y1
MY1
SHS
MSHS
MP1
CS
VSS
VDD
FD
MIN
MR
X
MX
PG
TX
R
VDD
VDD
VLP2
MLP2
VOUTR
Y2
MY2
SHR
MSHR
MP2
CR
VSS
VLN
MLN
VSS

Fig. 1(a)

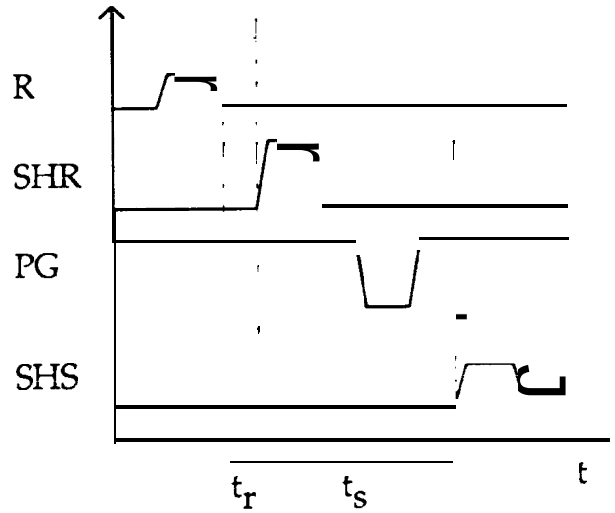

R
SHR
PG
SHS
t_r
t_s
t

Fig 1(b)

Table I

Transistor and Capacitor Sizes

E m	F	S ze
MR	In-pixel reset transistor	*3/2*
MIN	In-pixel source-follower input	6/2
MX	Row-selection switch	6/2
MLN	First source-follower load	*3/4*
MSHR, MSHS	Sample and hold switches	*3/'2*
MP1, MP2	Column source-follower inputs	*120/2*
MY I, MY2	Column-selection switches	120/2
MLP1, MLP2	Second source-follower loads	*30/2*
MCB	Crowbar switch	*3/2*
MS 1, MS2	Crowbar selection switches	*3/2*
CS, CR	Sample and hold capacitors	1 pF
CS, CR	Modified sample and hold capacitors	2.3 PF

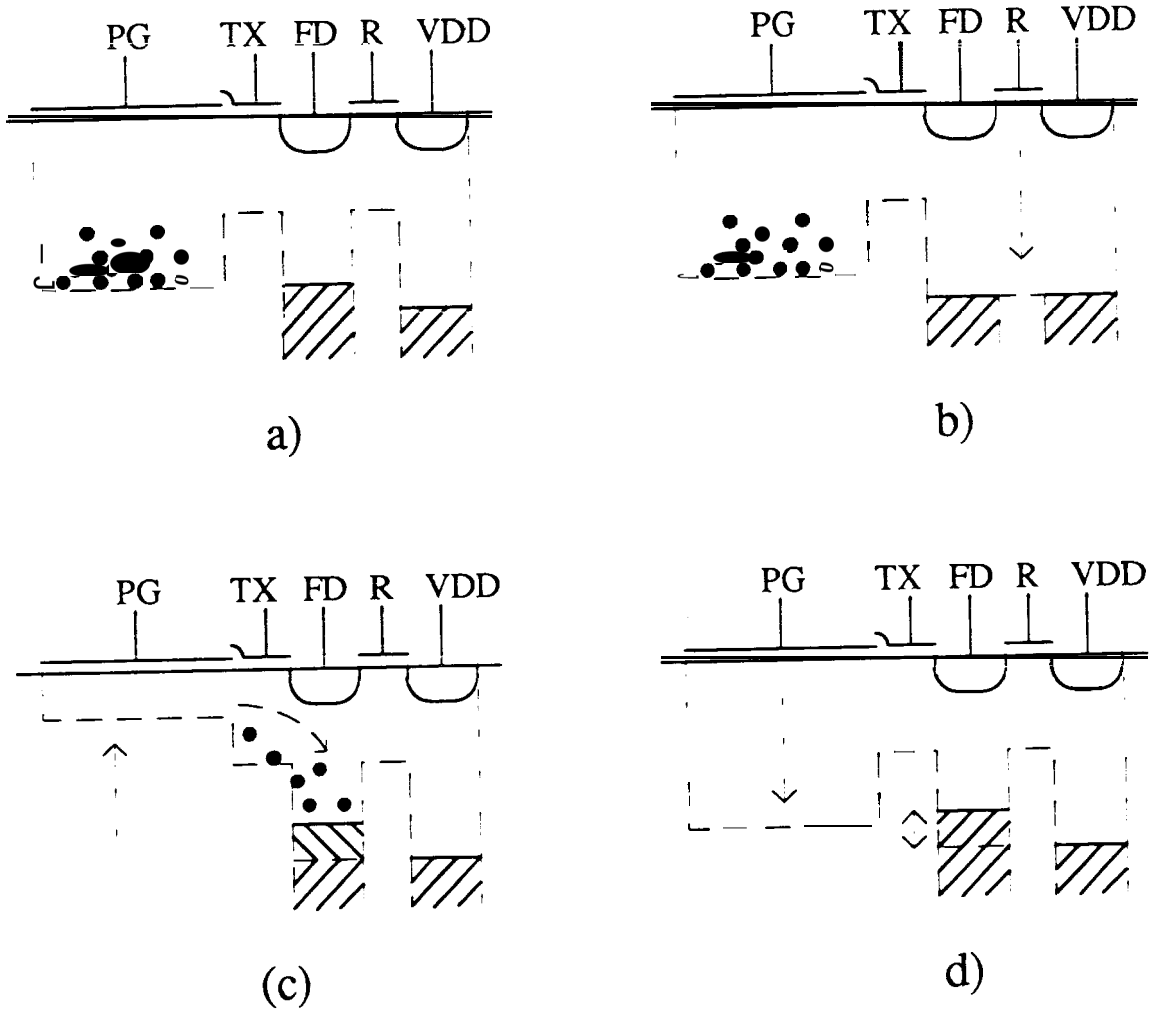
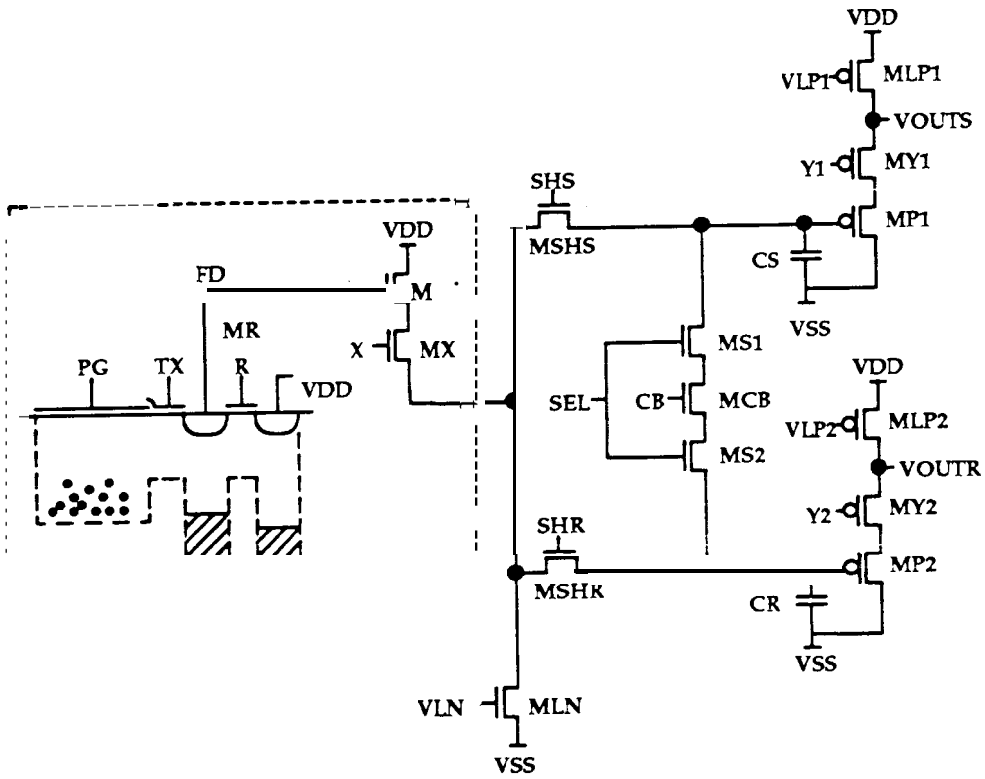


Fig. 2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VLP1
MLP1
VOUTS
Y1
MY1
SHS
MP1
MSHS
CS
VSS
VDD
FD
M
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MS1
PG
TX
R
VDD
SEL
CB
MCB
VDD
VLP2
MLP2
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Y2
MY2
SHR
MP2
MSHR
CR
VSS
VLN
MLN
VSS

Fig. 3(a)

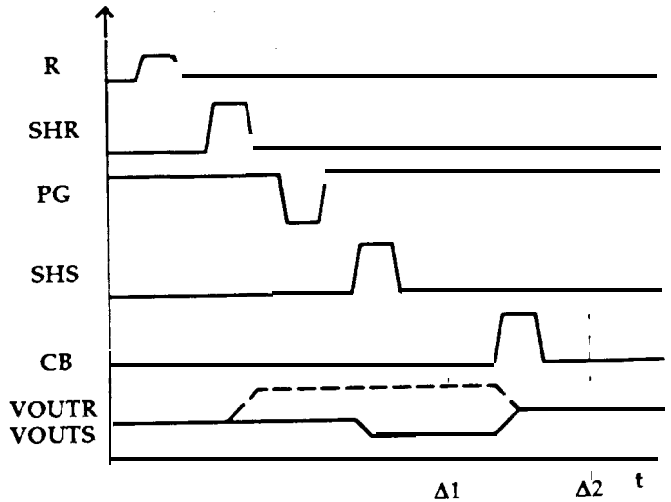
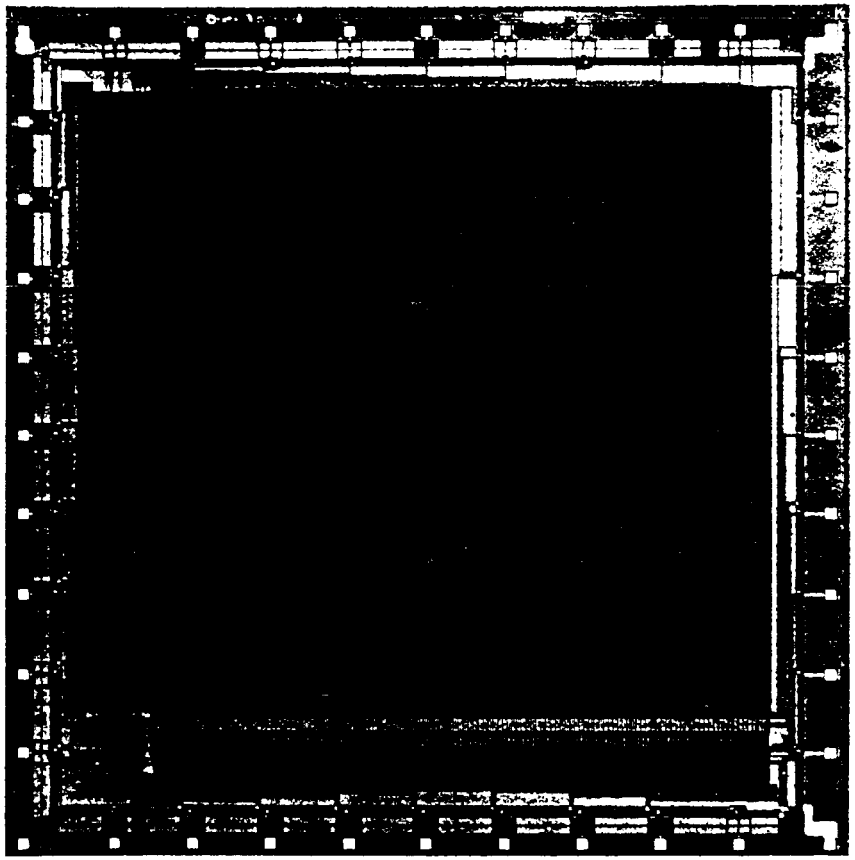

R
SHR
PG
SHS
CB
VOUTR
VOUTS
Δ1
Δ2
t

Fig.



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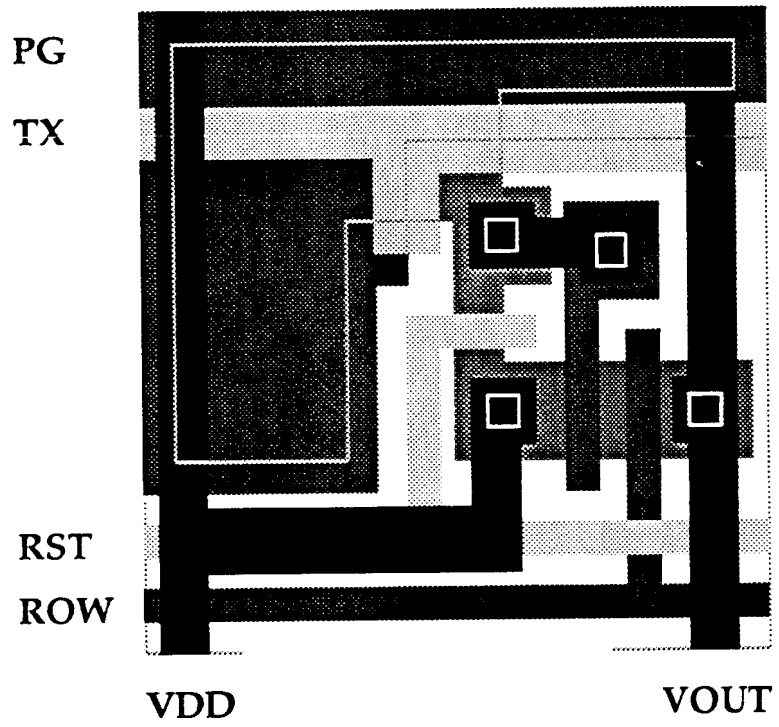

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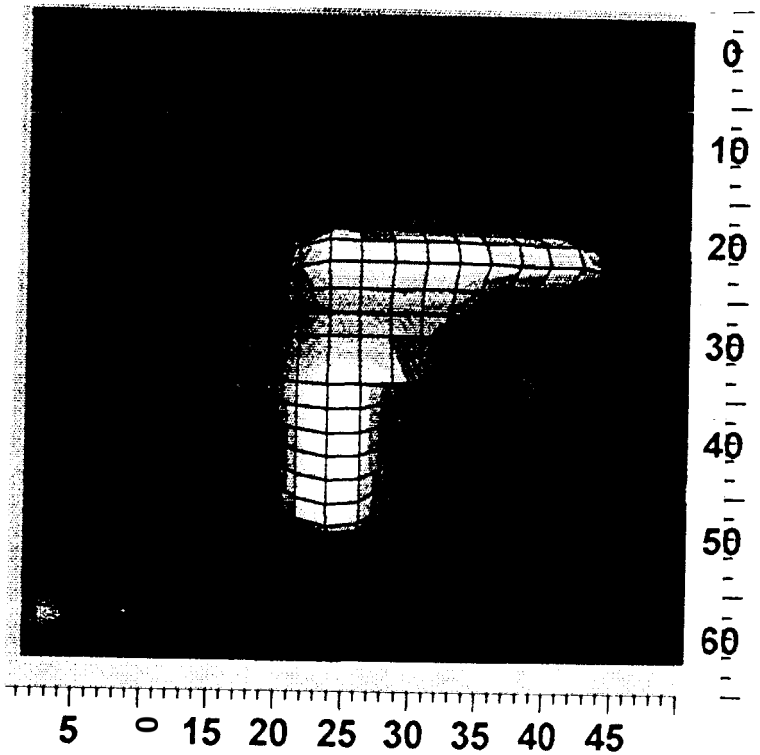
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30
40
50
60
5
0
15
20
25
30
35
40
45

Fig. 5(b)

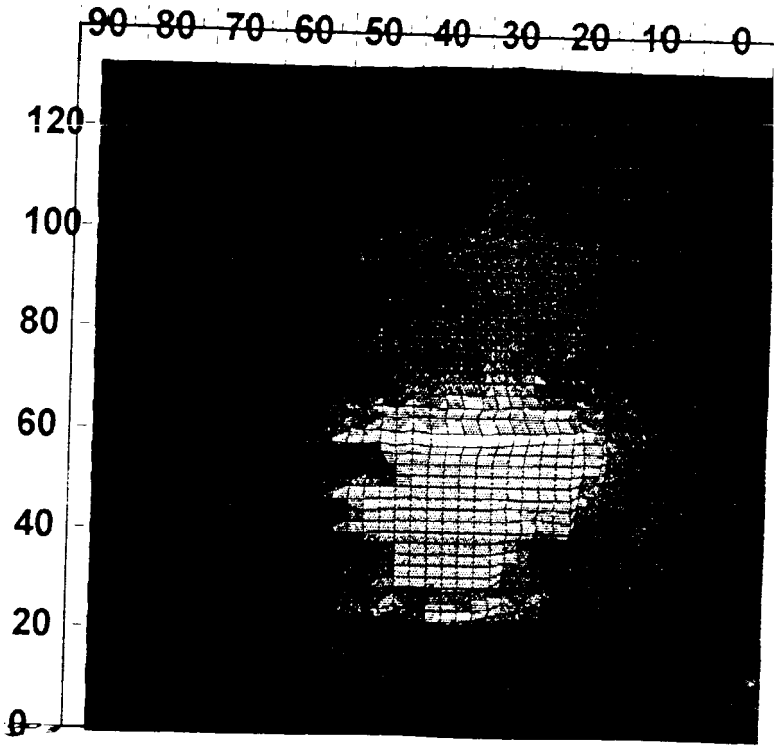

90
80
70
60
50
40
30
20
10
0
120
100
80
60
40
20
0

Fig. 5(c)

Fig. 6(a)

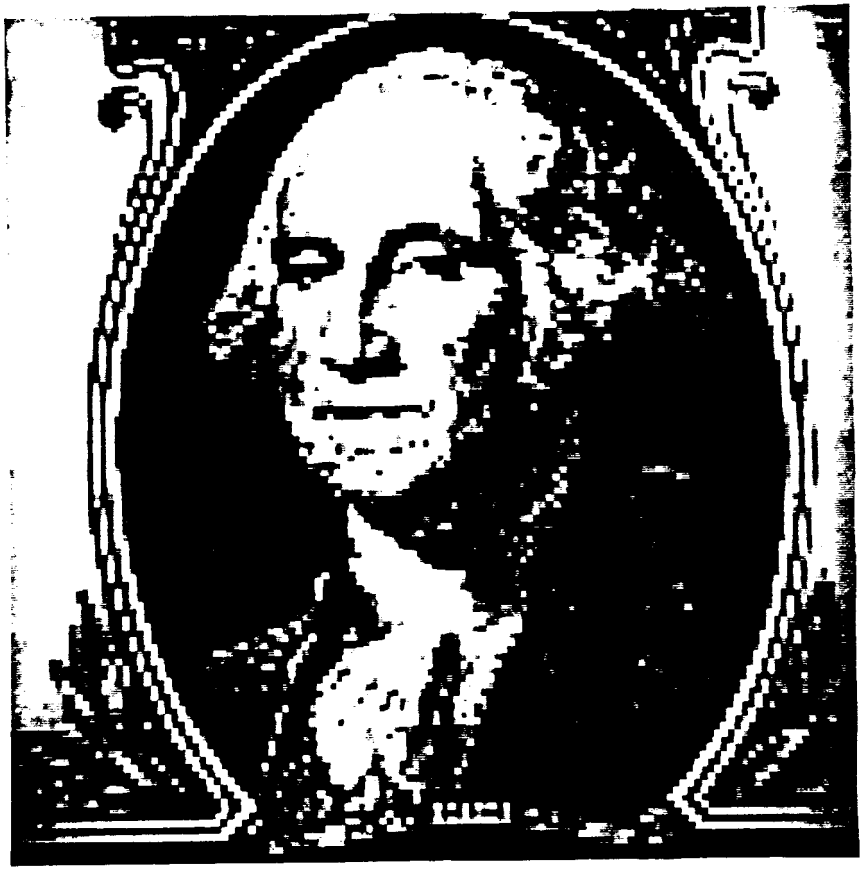
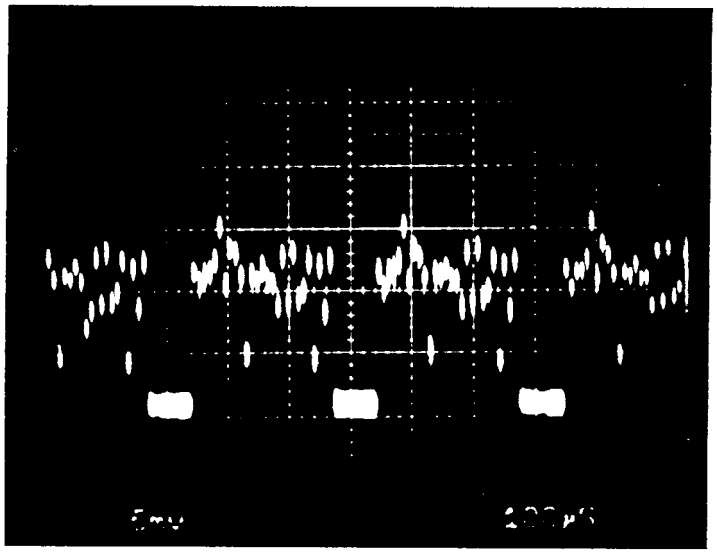


Fig. 6(b)



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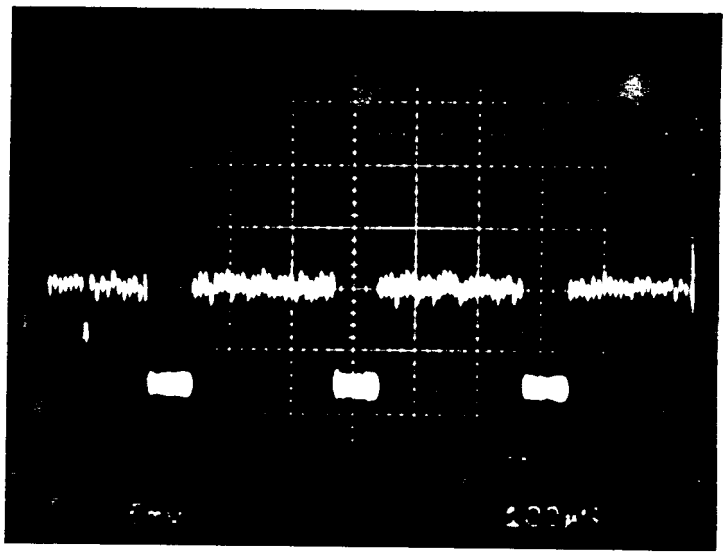

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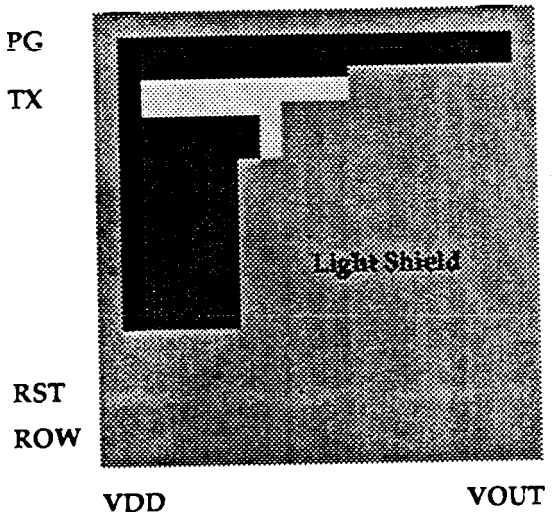

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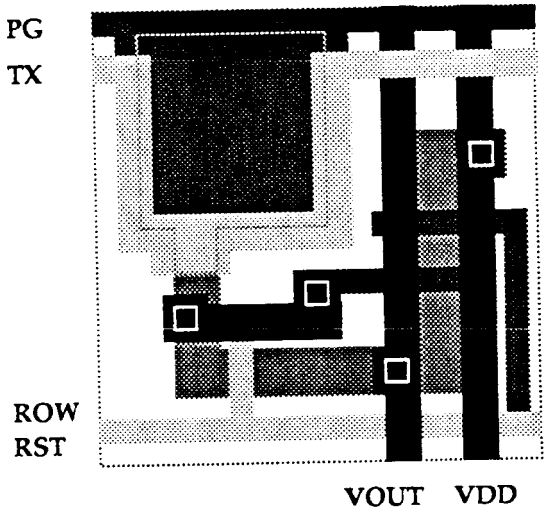

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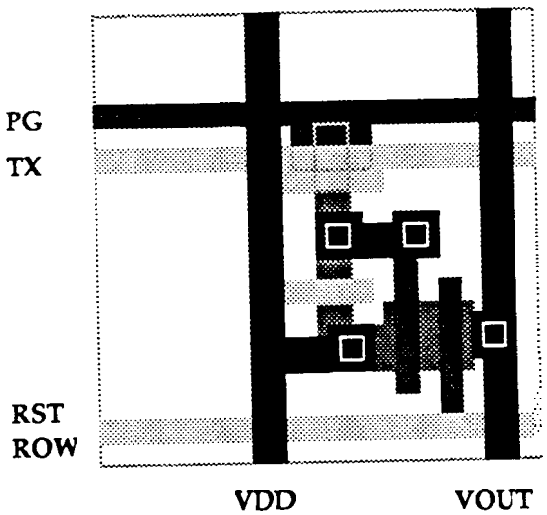

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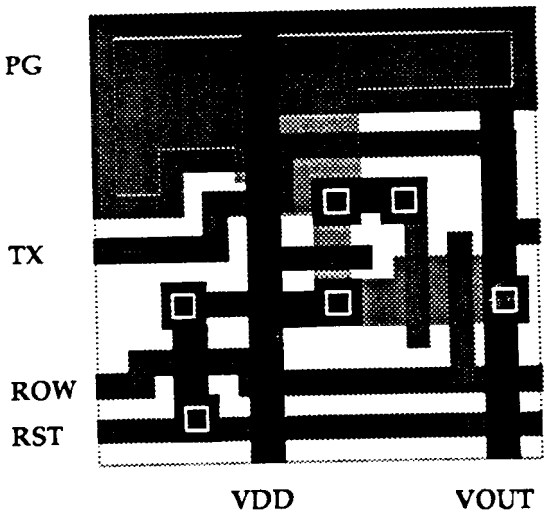

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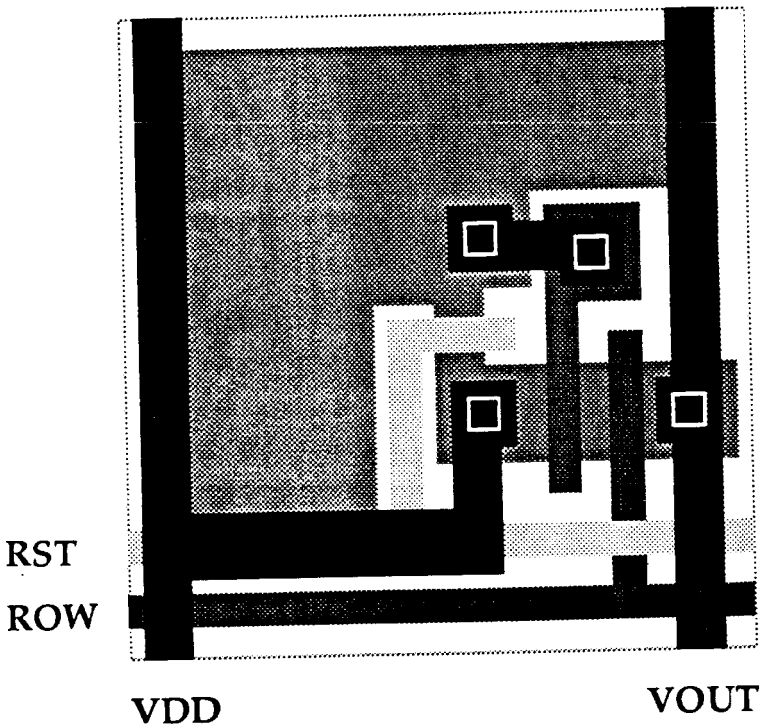

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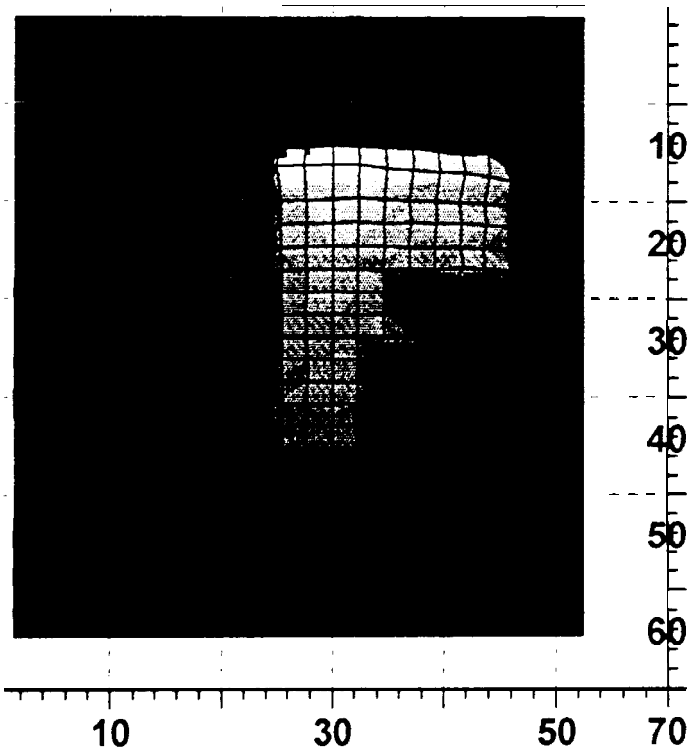

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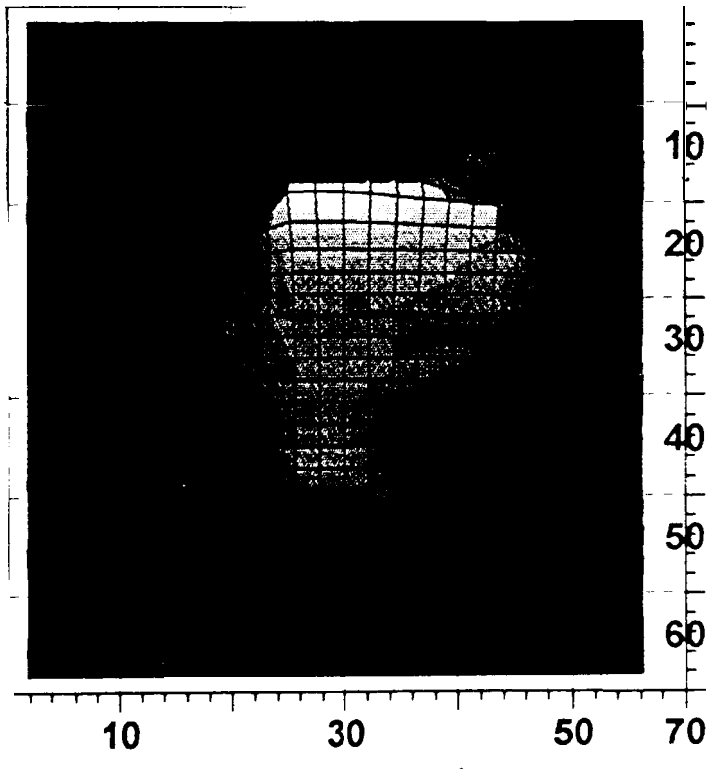

Fig. 9(c)

Table 11

summary of Experimental Results

Name	"Pixel Design	Process	Saturation (mV)	Sensitivity (pV/e⁻)	Relative Response	Noise* (μV)	Input Referred Noise (e-)	Dynamic Range (dB)	P-P FPN (mV)	Dark Current (V/s)
AR28P2	Baseline PG	P-well	*700*	3.3	0.26	160	*47*	73	26	
AR128P2	Baseline PG	P-well	600	3.7		153	*40*	72	20	0.26
AR128N2	Baseline PG	N-well	1200	6.5		209	*32*	75	30	1.76
AR28NCB	Crowbar	N-well	1300	7.1	1	197	*28*	76	1	1.16
AR128N5	Crowbar	N-well	1100	5.9		255	*43*	73	3	0.6
APSG2	Light-shielded	P-well	800	3.0		168	*55*	74		
APSG4	square PG	P-well	1000	3.1						
APSG7	Tiny PG	N-well	500	6.0	0.11	170	28	**69**		0.025
APSG1	Tiny PG	P-well	400	2.8		168	59	**68**		
APSG1O	Single poly PG	N-well	1000	7.1	1.09	180	25	**75**		0.34
APSG5	Photodiode	P-well	1300	2.1	1.48	177	83	77	7	0.22

*System noise:20 μV r.m.s.